What is claimed is:

1. A method of calibrating a non-volatile memory comprising:
reading a data state of a plurality of memory cells with a first sense amplifier;
reading the data state of the plurality of memory cells with a second sense amplifier;
comparing outputs of the first and second sense amplifiers to determine offsets between the first and second sense amplifiers; and
adjusting either the first or second sense amplifier to calibrate the first and second sense amplifiers.

2. The method of claim 1, wherein the first sense amplifier is used during erase and program operations.

3. The method of claim 1, wherein the second sense amplifier is used during read operations.

4. The method of claim 1, wherein the non-volatile memory is a flash memory.

5. The method of claim 1, wherein comparing the outputs of the first and second sense amplifiers is performed by an external test circuit.

6. The method of claim 1, wherein adjusting either the first or second sense amplifier comprises changing a voltage sensitivity of the sense amplifier.

7. A method of calibrating a non-volatile memory comprising:
storing a test pattern in the non-volatile memory;
reading the test pattern with a first read circuit;
reading the test pattern with a second read circuit;
outputting the read test pattern from the first and second read circuit to an external connection;

determining if an offset exists between the first and second read circuits; and adjusting either the first or second read circuit if an offset is determined.

8. The method of claim 7, wherein determining if an offset exists between the first and second read circuits further comprises utilizing an external tester to determine if an offset exists between the first and second read circuits.

9. The method of claim 7, wherein adjusting either the first or second read circuit if an offset is determined further comprises selectively adjusting voltage levels of either the first or second read circuit if an offset is determined.

10. The method of claim 7, wherein adjusting either the first or second read circuit if an offset is determined further comprises selectively adjusting read timing of either the first or second read circuit if an offset is determined.

11. The method of claim 7, further comprising selectively adjusting a verify circuit.

12. The method of claim 7, wherein the non-volatile memory is a flash memory.

13. A system comprising:
a memory test circuit; and
a non-volatile memory coupled to the memory test circuit comprising,
an array of memory cells,
a first read path having a first read circuit,
a second read path having a second read circuit, and
switch circuitry, wherein the switch circuitry is adapted to select the first or second read circuits and couple to the memory test circuit via external data connections.

14. The system of claim 13, wherein the memory test circuit is adapted to determine offset between the first and second read circuits.

15. The system of claim 14, wherein the non-volatile memory further comprises a control circuit, wherein the control circuit is adapted to adjust either the first or second read circuits in response to the memory test circuit.

16. A non-volatile memory comprising:
an array of memory cells;
a first read path having a first read circuit;
a second read path having a second read circuit; and
switch circuitry to select the first or second read circuits and couple to external data connections.

17. The non-volatile memory of claim 16, wherein the second read circuit comprises a verify circuit used during erase and program operations.

18. The non-volatile memory of claim 16, wherein the first read circuit comprises a read circuit used during read operations.

19. The non-volatile memory of claim 16, wherein the second read circuit comprises an adjustable verify sense amplifier circuit.

20. The non-volatile memory of claim 16, wherein the first read circuit comprises an adjustable read sense amplifier circuit.

21. The non-volatile memory of claim 16, wherein the switch circuitry is adapted to activate during a test operation to allow calibration testing between the first and second read circuits.